overcome the prior art references forming the 35 U.S.C. §103 rejections, but rather to overcome the Examiners objections and rejections under 35 U.S.C. §112. Therefore, the Applicant submits herewith a Request for Continued Examination (R.C.E.). EFS Form SB30 is submitted along with the appropriate fee.

CLAIM OBJECTIONS

In Paragraph 3 of the Detailed Action Section of your Office Action, the Examiner objected to appearances of the term "; and,". The Applicant fails to understand the objection. However, he has amended claims 7, 11, and 14 to delete the comma following the word "and."

CLAIM REJECTIONS – 35 U.S.C. §112

In Paragraph 5 of the Detailed Action Section of your Office Action, the Examiner rejected claims 11-13, and 17 under 35 U.S.C. §112, first paragraph as failing to comply with the written description requirement. Accordingly, the Applicant has amended claims 7, 11, 12, and 17 to overcome the Examiner's rejections. The Applicant respectfully requests that the Examiner reverse her 35 U.S.C. §112 rejections in light of these amendments.

CLAIM REJECTIONS – 35 U.S.C. §103

In Paragraph 6 of the Detailed Action Section of your Office Action, the Examiner rejected all pending claims under 35 U.S.C. §103(a) as being unpatentable over US Patent No. 6,088,008 (hereinafter Reeder) in view of Japanese Patent Publication No. 05-173499 (hereinafter Atuso). Accompanying your Office Action was a computerized translation of the Japanese text of Atuso into English. Since you have supplied this translation to the Applicant, the Applicant presumes that said translation accurately describes the Atuso invention, and he relies thereon.

TRAVERSING ARGUMENTS

Paragraph 7 of the Detailed Action Section of your Office Action is concerned with the rejection of claim 7 of the Present Application. At the end of Paragraph 7, the Examiner alleged that it would have been obvious to a person having ordinary skill in the art at the time of the filing of the Present Application to

modify the teachings of Reeder and to combine into them the teachings of Atuso to produce the Present Invention.

First, it is not possible to combine the teachings of Reeder with the teachings of Atuso. Reeder's FIG 2 demonstrates the concept of his invention. Reeder uses individual display units (521, 522, 523, …, 524) to each display a single character (CHAR1, CHAR2, CHAR3, …, CHARn, respectively). From his controller, 518, an individual data line extends to each display unit (531, 532, 533, …, 534, respectively). Therefore, addressing the individual display units is not required, because each character display unit is directly wired. The data sent to each display unit contains a small matrix of data to operate a standard ASCII generator that lights up each display. Within each display unit is a matrix reader for the ASCII generator, which drives the display lamps. Each individual display lamp has an X-Y address. However, the display units themselves have no addresses as they are directly wired. In FIG. 1, in order to display "DRIVE CAREFULLY," the 'D' is transmitted directly on a dedicated wire to unit (1,3), the 'R' is transmitted to unit (1,4), the 'I' is transmitted to unit (1,5), *etc.* Following this concept, the final 'Y' in the word "CAREFULL**Y**" is transmitted to the character display unit located at position (2,9). These foregoing X-Y coordinates are not addressed by Reeder, but rather, illustrative of the positions of the character display units in the drawing of FIG. 1. The only addressing used by Reeder belongs to the ASCII matrix for each character, which is done only within the character generator in each unit.

Atuso does not directly address each individual unit. He sends an X-Y matrix on X and Y parallel data busses. In Drawing 2, elements 6a and 6b show an X and Y configuration of parallel data to receiver unit 5 (not described). It also shows data lines 2 and 3 as an X and Y input and line 4 as a serial line-in and line-out. Drawing 1 shows lines 2 and 3 as X and Y input of data going to each of the individual units indicated by their X-Y coordinates. This requires that the data be presented to each unit as X-Y data to be latched.

Reeder requires his data to be sent from the controller to each display unit by a separate unique data wire. Atuso only uses two wires of his controller to

send X and Y data, one display at a time, followed by a latching address via wire 4. All the lines are then cleared for the next X-Y matrix. This process is repeated until all the data has been sent, and the last latch has been cleared.

Reeder and Atuso represent two completely different and incompatible systems for sending data to individual modules. Reeder cannot possibly use a self-addressing control unit system as alleged by the Examiner. The impossibility of combining Reeder and Atuso into a single system renders the Present Invention non-obvious over the prior art.

Second, the Examiner alleged similarity of the Present Invention to Reeder in Page 6, sub-paragraphs (a) through (d), and (f), and indicates what Reeder does not teach in sub-paragraphs (e) and (g). She then alleged similarity of the Present Invention to Atuso in Page 7, sub-paragraphs (a), (e), (d), and (g). The Applicant disagrees with the Examiner in her descriptions in sub-paragraphs (e), (d), and (g).

- Nowhere does Atuso teach receiving an address from a previous control unit, nor does he teach a transmitter to send an address to the next control unit. He does teach that his controller will send all of the address data as serial data via serial line 4 and each display panel will latch the binary number and allow all the other binary numbers to pass onto the next unit until all of the panel latches are filled.
- Nowhere does Atuso teach that his display panels permanently store their addresses in non-volatile memory.

Third, Atuso does not teach that his panels can accept arbitrary data within data packets that are in random order. He only teaches that the data coming down lines 2 and 3 must be present and available in sequential order, and must wait until serial data line 4 sends the address to be latched before sending the next packet of data. This is a significant difference between Atuso and the Present Invention. As will be seen shortly, this produces unexpected results.

Clearly, the Present Invention is entirely different from Reeder in that the Present Invention requires only one data line to address all of the Present Application's plurality of control units.

In the Present Application, FIG. 4 (described in the Specification, Page 14, lines 5-12) and FIG. 5 (described on Page 14, lines 13-17) both show prior art circuitry. Atuso cleverly combined the circuitry of FIG. 4 with that of FIG. 5. Atuso's similarity to FIG. 4 can be seen by observing his Drawing 1. In FIG. 4 of the Present Application, there is a BCD standard transmission schematic. Under the lines, there are two latches to capture the BED data in order with the clock pulses. In Atuso's Drawing 1, there are two BCD transmitters, 2 and 3, which provides eight data lines instead of four. Atuso replaces the global clock of FIG. 4 with a serial data clock as in FIG. 5. This allows him to have an addressable clock pulse, which controls each latch sequentially along line 4. Every time a packet of data is sent, a timing control pulse (seen also in FIG. 4) must be sent in order for the data to be latched. Atuso, by replacing the clock with serial pulses, the data latching will progress to the next latch until the last module is addressed. Then the latches will all be reset to accept the next packet of data. With this type of system (as described in the Present Application on Page 14, lines 16-17), if one of the units malfunctions, no succeeding unit will be able to latch its data. This is a significant disadvantage of the Atuso invention.

The Present Invention, as shown in Figures 6 and 7, does not depend on a serial addressing line or a BCD packet line to tell a control unit when to capture its data. Instead, because each unit permanently stores its address after initialization, it never needs to refresh the data or the clock pulse unless there is a malfunction in that unit. The address line is only used once to send a single address (usually '0') to the first unit on the address line. That first unit adds '1' to form its own address, stores that address, and then sends it on a separate line to the next unit in sequence. Each unit addresses itself.

In the Present Invention, a single stream of data consists of a plurality of data packets – one data packet for each control unit. Each packet comprises the address of the intended control unit and the data, which that unit requires for

processing. All units receive all of the data, but any single unit will process only that packet intended for it. The data packets may be sent in any random order. The units can be addressed as needed without requiring sequential transmission to each of the units. No clock pulse is required. Atuso requires serial transmission along with a clock pulse.

In the Present Invention, when a unit malfunctions, all other units (both preceding and succeeding) still maintain their addresses and data (even in the event of a power failure). Because a clock pulse is not required, all the remaining working units receive the same data and use their permanently stored addresses to process the data intended for them. When the defective unit is replaced, the replaced unit knows that it has no address. It then broadcasts through the global feedback line to the key module, requesting that the key module send an addressing pulse to all the units. In this way, the entire system re-addresses itself.

This is a unique feature not present in Atuso, and the results realized by the Present Invention are unexpected. Therefore, the Present Invention is not obvious over Reeder, Atuso, or any combination of the two.

Independent claim 7, as presently amended, recites the system as described above. Therefore, the Applicant respectfully requests that the Examiner reverse her rejection of claim 7 as being obvious over Reeder in view of Atuso.

Claims 8-13, and 17 depend either directly or indirectly from claim 7. If claim 7 proves to be allowable, so also must dependent claims 8-13 as they incorporate all of the limitations of claim 7 by reference therein.

Regardless, as per claim 10, Reeder does not teach that each control unit includes a non-volatile memory, which stores the address of the control unit. Reeder's control units do not use an address. The only addressing in Reeder's units is the lamp ASCII circuitry that forms the display character. This is an irrelevant element.

Independent claim 14 recites an individual control unit. Contrary to the Examiner's assertions in Paragraph 14 the Detailed Action Section of your Office

Action, Reeder does not teach a self-addressing control unit. Reeder's display units do not have an address, and they do no self address. They are hard wired into the controller. Reeder's control units do not comprise:

a) "a transmission receiver (*i.e.,* logic circuit) that receives an address" from a first other control unit in the system; or

c) "memory storage that stores its new address of the control unit."

The only addressing is that of the lamps in the character display and not that of the control unit itself.

As was discussed previously, Atuso does not teach a control unit that either receives an address from a preceding control unit in the system and calculates and stores a new address nor a transmitter that sends its new address to a succeeding control unit.

Even if one can pick and choose elements of Reeder and Atuso and attribute them to elements in claim 14, as discussed *supra*, it is impossible to combine Reeder and Atuso to produce the Present Invention. For claim 14 to be obvious over Reeder in view of Atuso, it must have been possible for Reeder to incorporate the missing elements of Atuso into his own invention to produce the Present Invention. This not being the case renders claim 14 non-obvious.

Claims 15 and 16 depend directly from claim 14. If claim 14 is allowable, so also must claims 15 and 16 be allowable, since they incorporate the limitations of claim 14 by reference therein.

Finally, independent claim 18 is a method claim. Referring to Paragraph 18 of the Detailed Action Section of your Office Action, as discussed *supra*, Atuso does not teach:

> *"causing each control unit to calculate an address associated with that control unit … by receiving an initial address from a first other control unit …, performing a mathematical operation on that address to create a new address …, and transmitting the new address to a second other control unit;" or*
>
> *"self-configuring and automatic set-up of a control unit … via the control unit addressing itself in the system by receiving an initial address from a previous or prior control unit, … performing the mathematical operation on that initial address to produce a new address."*

The detailed addressing and data transmission scheme of Atuso was discussed previously.

Furthermore, because it is impossible to combine the teachings of Reeder and Atuso, the Examiner was picking and choosing elements of disparate prior art references to impermissibly reject claim 18 under 35 U.S.C. §103(a). Here, the cited elements from Reeder and Atuso are inconsistent with each other. Therefore, the method invention recited in claim 18 cannot be deemed obvious over these prior art references.

REQUEST FOR RECONSIDERATION AND REVERSAL OF REJECTIONS

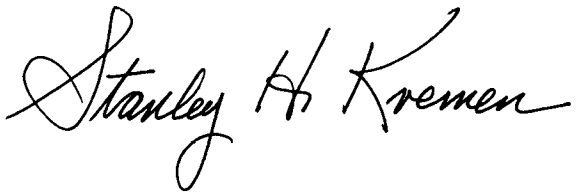
Based upon the foregoing traversal arguments and accompanying claim amendments, the Applicant respectfully requests that the Examiner reverse her rejections and objections, and allow the entire application.

APPLICANT'S ATTEMPT TO PROVIDE A COMPLETE RESPONSE

By submitting this reply to your Office Action, the Applicant has made a good faith effort to respond to every ground of rejection and objection put forth by the Examiner. However, should this reply be deficient in any respect, since time remains for reply, the Applicant would appreciate the courtesy of an Advisory Office Action that would permit him to correct any deficiency.

Thank you for your kind attention.

Respectfully submitted,



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